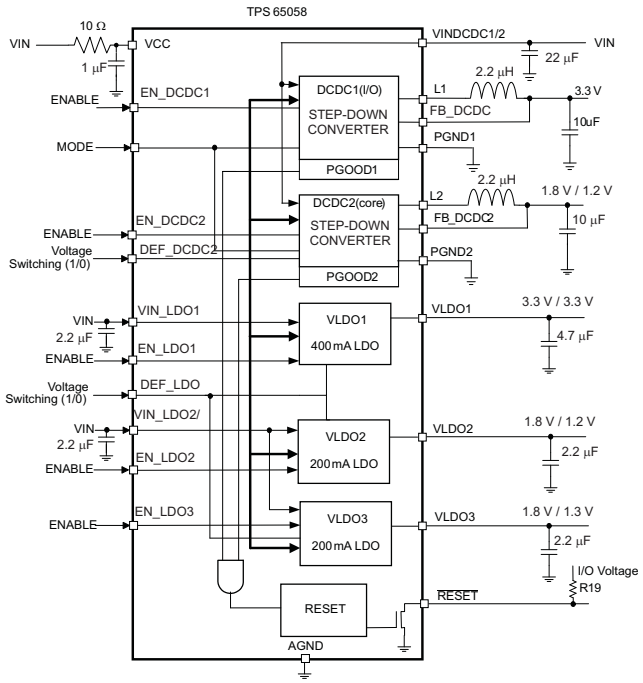
2.25 MHz Dual STEP DOWN CONVERTER WITH 3 LOW-INPUT VOLTAGE LDOs

FEATURES

- Up To 95% Efficiency
- Output Current for DC/DC Converters:
  - DCDC1 = 0.6A; DCDC2 = 1A
- V_{IN} Range for DC/DC Converters From 2.5V to 6V
- Dynamic Voltage Switching for Processor Core Supply Supported
- 2.25MHz Fixed Frequency Operation
- Power Save Mode at Light Load Current
- 180° Out-of-Phase Operation
- Output Voltage Accuracy in PWM mode ±1%
- Total Typical 32μA Quiescent Current for Both DC/DC Converters
- 100% Duty Cycle for Lowest Dropout
- One General-Purpose 400mA LDO
- Two General-Purpose 200mA LDOs
- V_{IN} Range for LDOs from 1.5V to 6.5V
- Reset Generator and Power Monitor
- Available in a 4 mm x 4 mm 24-Pin QFN Package

APPLICATIONS

- Satellite Radio Modules



NOTE: Other voltage options available upon request. Contact your Texas Instruments representative.

DESCRIPTION

The TPS65058 is an integrated Power Management IC for applications powered by one Li-Ion or Li-Polymer cell, which require multiple power rails. The TPS65058 provides two highly efficient, 2.25MHz step down converters targeted at providing the core voltage and I/O voltage in a processor based system. Both step-down converters enter a low power mode at light load for maximum efficiency across the widest possible range of load currents. For low noise applications, the devices can be forced into fixed frequency PWM mode by pulling the MODE pin high. Both converters allow the use of small inductors and capacitors to achieve a small solution size. TPS65058 provides an output current of up to 0.6A on the DCDC1 converter, and up to 1A on the DCDC2 converter. The TPS65058 also integrates one 400mA LDO and two 200mA LDO voltage regulators, which can be turned on/off using separate enable pins on each LDO. Each LDO operates with an input voltage range between 1.5V and 6.5V allowing them to be supplied from one of the step down converters or directly from the main battery.

The TPS65058 comes in a small 24-pin leadless package (4mm × 4mm QFN) with a 0,5mm pitch.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION(1)

T_A	PART NUMBER	QFN(2) PACKAGE	PACKAGE MARKING
–40°C to 85°C	TPS65058	RGE	65058

(1) For the most current package and ordering information, see the *Package Option Addendum* at the end of this document, or see the TI web site at www.ti.com.
(2) The RGE package is available in tape and reel. Add R suffix (TPS65058RGER) to order quantities of 3000 parts per reel. Add T suffix (TPS65058RGET) to order quantities of 250 parts per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNITS
V_I	Input voltage range on all pins except AGND, PGND, and EN_LDO1 pins with respect to AGND	–0.3 V to 7 V
	Input voltage range on EN_LDO1 pin with respect to AGND	–0.3 V to V_{CC} + 0.5 V
I_I	Current at VINDCDC1/2, L1, PGND1, L2, PGND2	1800 mA
	Current at all other pins	1000 mA
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature	–40°C to 85°C
T_J	Maximum junction temperature	125°C
T_{stg}	Storage temperature range	–65°C to 150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	$R_{\theta JA}$	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
RGE	35 K/W	2.8 W	28 mW/K	1.57 W	1.14 W

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
$V_{INDCDC1/2}$	Input voltage range for step-down converters	2.5		6	V
V_{DCDC1}	Output voltage range for VDCDC1 step-down converter		3.3		V
V_{DCDC2}	Output voltage range for VDCDC2 step-down converter (DEF_DCDC2 = 1/0)		1.8/1.2		V
V_{INLDO1}, $V_{INLDO2/3}$	Input voltage range for LDOs	1.5		6.5	V
V_{LDO1}	Output voltage range for LDO1 (DEF_LDO = 1/0)		3.3/3.3		V
V_{LDO2}	Output voltage range for LDO2 (DEF_LDO = 1/0)		1.8/1.2		V
V_{LDO3}	Output voltage for LDO3 (DEF_LDO = 1/0)		1.8/1.3		V
$I_{OUTDCDC1}$	Output current at L1			600	mA
L1	Inductor at L1 (1)	1.5	2.2		µH
$C_{INDCDC1/2}$	Input capacitor at $V_{INDCDC1/2}$ (1)	22			µF
$C_{OUTDCDC1}$	Output capacitor at V_{DCDC1} (1)	10	22		µF
$I_{OUTDCDC2}$	Output current at L2			1000	mA
L2	Inductor at L2 (1)	1.5	2.2		µH
$C_{OUTDCDC2}$	Output capacitor at V_{DCDC2} (1)	10	22		µF
C_{VCC}	Input capacitor at VCC (1)	1			µF
C_{in1-2}	Input capacitor at VINLDO1, VINLDO2/3 (1)	2.2			µF
C_{OUT1-2}	Output capacitor at VLDO1-3 (1)	2.2			µF
I_{LDO1}	Output current at LDO1			400	mA
I_{LDO2}	Output current at LDO2			230	mA
I_{LDO3}	Output current at LDO3			200	mA
T_A	Operating ambient temperature range	–40		85	°C
T_J	Operating junction temperature range	–40		125	°C
R_{CC}	Resistor from battery voltage to V_{CC} used for filtering (2)		1	10	Ω

(1) See the *Application Information* section of this data sheet for more details.
(2) Up to 2 mA can flow into V_{CC} when both converters are running in PWM, this resistor causes the UVLO threshold to be shifted accordingly.

ELECTRICAL CHARACTERISTICS

V_{cc} = VINDCDC1/2 = 3.6V, EN = V_{cc}, MODE = GND, L = 2.2µH, C_{OUT} = 22µF, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT							
V_{cc}	Input voltage range			2.5		6.	V
I_Q	Operating quiescent current Total current into V_{CC}, VINDCDC1/2, VINLDO1, VINLDO2/3		One converter, I_{OUT} = 0 mA.PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = Vin OR EN_DCDC2 = Vin; EN_LDO1= EN_LDO2 = EN_LDO3 = GND		20	30	µA
			Two converters, I_{OUT} = 0 mA, PFM mode enabled (Mode = 0) device not switching, EN_DCDC1 = Vin AND EN_DCDC2 = Vin; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND		32	40	µA
			One converter, I_{OUT} = 0 mA, PFM mode enabled (Mode = GND) device not switching, EN_DCDC1 = Vin OR EN_DCDC2 = Vin; EN_LDO1 = EN_LDO2 = EN_LDO3 = Vin		145	210	µA
I_Q	Operating quiescent current into V_{CC}		One converter, I_{OUT} = 0 mA, Switching with no load (Mode = Vin), PWM operation EN_DCDC1 = Vin OR EN_DCDC2 = Vin; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND		0.85		mA
			Two converters, I_{OUT} = 0 mA, Switching with no load (Mode = Vin), PWM operation EN_DCDC1 = Vin AND EN_DCDC2 = Vin; EN_LDO1 = EN_LDO2 = EN_LDO3 = GND		1.25		mA
$I_{(SD)}$	Shutdown current		EN_DCDC1 = EN_DCDC2 = GND EN_LDO1 = EN_LDO2 = EN_LDO3 = GND		9	12	µA
$V_{(UVLO)}$	Undervoltage lockout threshold for DCDC converters and LDOs		Voltage at V_{CC}		1.8	2	V
EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, MODE							
V_{IH}	High-level input voltage MODE, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, DEF,DEF_LDO,DEF_DCDC2			1.2		V_{CC}	V
V_{IL}	Low-level input voltage MODE, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, DEF_LDO, DEF_DCDC2			0		0.4	V
I_{IN}	Input bias current MODE, EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3, DEF_LDO, DEF_DCDC2		MODE = GND or VIN		0.01	1	µA
POWER SWITCH							
$r_{DS(on)}$	P-channel MOSFET on resistance	DCDC1, DCDC2	VINDCDC1/2 = 3.6V		250	350	mΩ
			VINDCDC1/2 = 2.5V		380	500	
I_{LD_PMOS}	P-channel leakage current		$V_{(DS)}$ = 6V			1	µA
$r_{DS(on)}$	N-channel MOSFET on resistance	DCDC1, DCDC2	VINDCDC1/2 = 3.6V		180	250	mΩ
			VINDCDC1/2 = 2.5V		250		
I_{LK_NMOS}	N-channel leakage current		$V_{(DS)}$ = 6V		7	10	µA
$I_{(LIMF)}$	Forward Current Limit PMOS (High-Side) and NMOS (Low side)	DCDC1	2.5V ≤ V_{IN} ≤ 6V	1.19	1.4	1.65	A
		DCDC2		0.85	1.0	1.15	
T_{SD}	Thermal shutdown		Increasing junction temperature		150		°C
	Thermal shutdown hysteresis		Decreasing junction temperature		20		°C
OSCILLATOR							
f_{SW}	Oscillator frequency			2.025	2.25	2.475	MHz

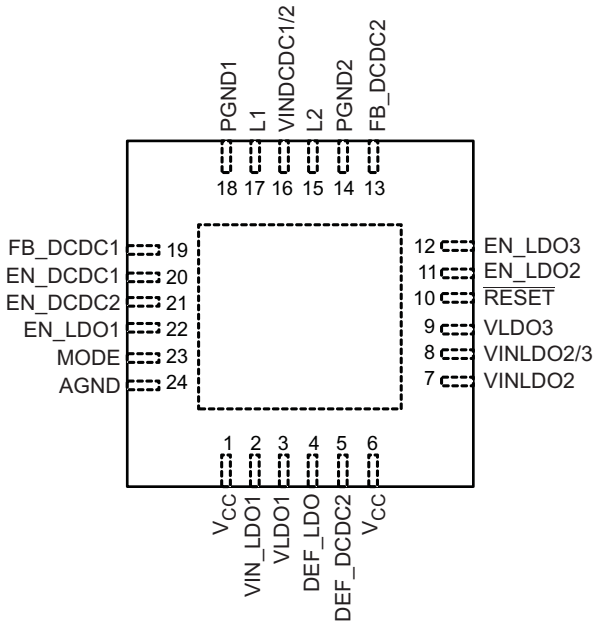
ELECTRICAL CHARACTERISTICS (continued)

V_{cc} = VINDCDC1/2 = 3.6V, EN = V_{cc}, MODE = GND, L = 2.2µH, C_{OUT} = 22µF, T_A = –40°C to 85°C typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT							
V_{OUT}	DC output voltage accuracy	DCDC1, DCDC2	V_{IN} = 2.5V to 6V, Mode = GND, PFM operation, 0 mA < I_{OUT} < I_{OUTMAX}	-2%	0	2%	
			V_{IN} = 2.5V to 6V, Mode = V_{IN}, PWM operation, 0 mA < I_{OUT} < I_{OUTMAX}	–1%	0	1%	
ΔV_{OUT}	Power save mode ripple voltage		I_{OUT} = 1mA, Mode = GND, V_O = 1.3V, Bandwidth = 20MHz		25		mV_{PP}
t_{Start}	Start-up time		Time from active EN to Start switching		170		µs
t_{Ramp}	V_{OUT} Ramp up Time		Time to ramp from 5% to 95% of V_{OUT}		750		µs
	$\overline{RESET}$ delay time		Input voltage at threshold pin rising	80	100	120	ms
V_{OL}	$\overline{RESET}$ output low voltage		I_{OL} = 1mA			0.2	V
	$\overline{RESET}$ sink current				1		mA
	$\overline{RESET}$ output leakage current				10		nA
VLDO1, VLDO2, VLDO3 LOW DROPOUT REGULATORS							
V_{INLDO}	Input voltage range for LDO1, LDO2, LDO3			1.5		6.5	V
V_{LDO1}	LDO1 output voltage range (DEF_LDO = 1/0)				3.3/3.3		V
V_{LDO2}	LDO2 output voltage range(DEF_LDO = 1/0)				1.8/1.2		V
V_{LDO3}	LDO3 output voltage (DEF_LDO = 1/0)				1.8/1.3		V
$V_{(FB)}$	Feedback voltage for FB_LDO1, FB_LDO2				1		V
I_O	Maximum output current for LDO1			400			mA
	Maximum output current for LDO2			230			mA
	Maximum output current for LDO3			200			mA
$I_{(SC)}$	LDO1 short-circuit current limit		V_{LDO1} = GND			850	mA
	LDO2 and LDO3 short-circuit current limit		V_{LDO2} = GND, V_{LDO3} = GND			420	mA
	Dropout voltage at LDO1		I_O = 400mA, V_{INLDO1} = 1.8V			280	mV
	Dropout voltage at LDO2, LDO3		I_O = 200mA, VINLDO = 1.8V			280	mV
	Output voltage accuracy for LDO1, LDO2, LDO3		I_O = 10mA	–2%		1%	
	Line regulation for LDO1, LDO2, LDO3		$V_{INLDO1,2}$ = $V_{LDO1,2}$ + 0.5V (min. 2.5V) to 6.5V, I_O = 10 mA	–1%		1%	
	Load regulation for LDO1, LDO2, LDO3		I_O = 0mA to 400mA for LDO1 I_O = 0mA to 230mA for LDO2 I_O = 0mA to 200mA for LDO3	–1%		1%	
	Regulation time for LDO1, LDO2, LDO3		Load change from 10% to 90%		10		µs
PSRR	Power supply rejection ratio		f = 10kHz; I_O = 50mA; V_I = V_O + 1 V		70		dB
$R_{(DIS)}$	Internal discharge resistor at VLDO1, VLDO2, VLDO3		Active when LDO is disabled		300		Ω
T_{SD}	Thermal shutdown		Increasing junction temperature		140		°C
	Thermal shutdown hysteresis		Decreasing junction temperature		20		°C

PIN ASSIGNMENTS

RGE PACKAGE
(TOP VIEW)



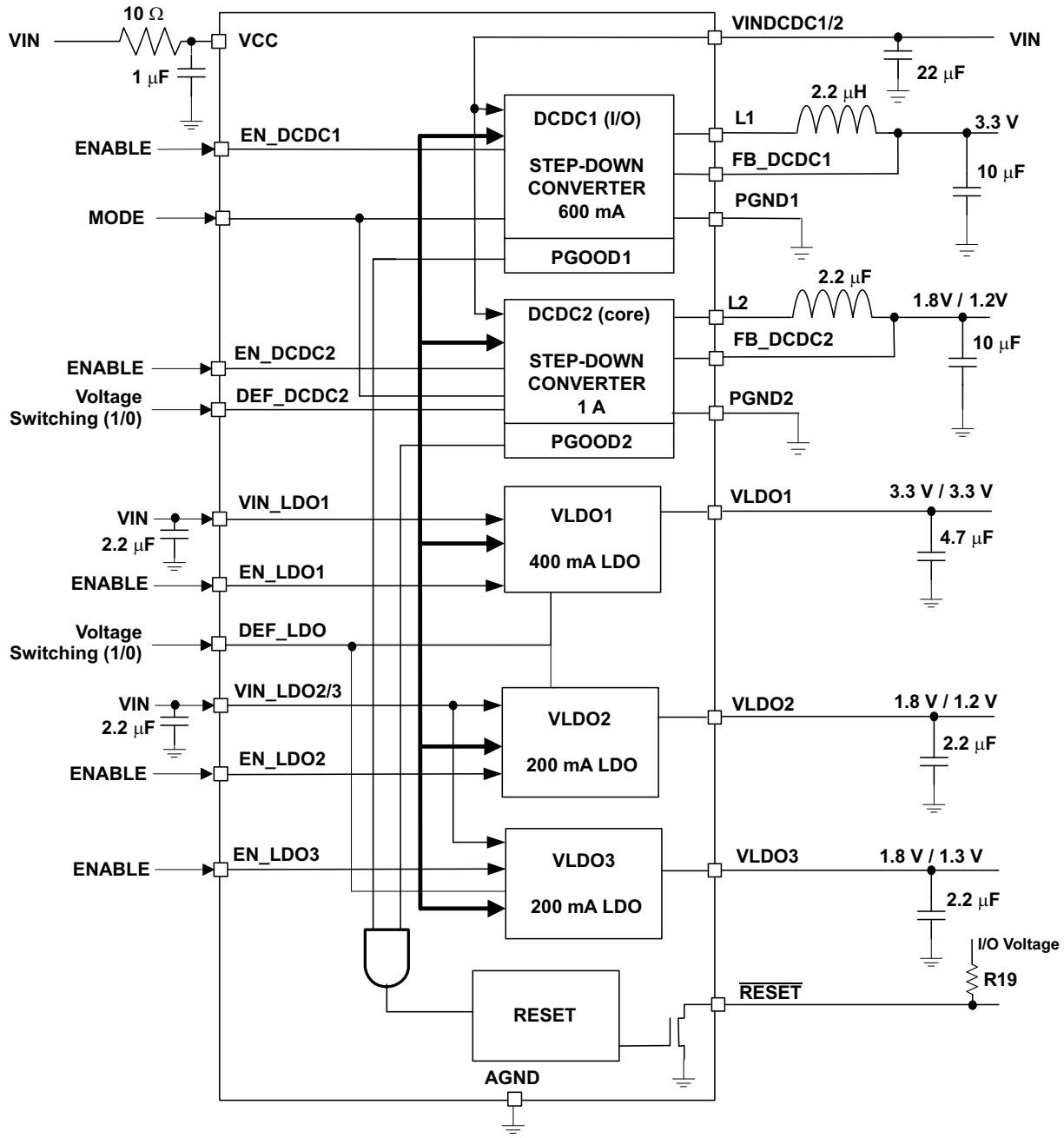
TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
V_{CC}	1, 6	I	Power supply for digital and analog circuitry of DCDC1, DCDC2 and LDOs. This pin must be connected to the same voltage supply as VINDCDC1/2.
FB_DCDC1	19	I	Feedback input for DCDC1
MODE	23	I	Select between Power Safe Mode and forced PWM Mode for DCDC1 and DCDC2. In Power Safe Mode PFM is used at light loads, PWM for higher loads. If PIN is set to high level, forced PWM Mode is selected. If Pin has low level, then Device operates in Power Safe Mode.
VINDCDC1/2	16	I	Input voltage for VDCDC1 and VDCDC2 step-down converter. This must be connected to the same voltage supply as V_{CC}.
FB_DCDC2	13	I	Feedback input for DCDC1
L1	17	O	Switch pin of converter 1. Connected to Inductor
PGND1	18	I	GND for converter 1
PGND2	14	I	GND for converter 2
AGND	24	I	Analog GND, connect to PGND and PowerPAD™
L2	15	O	Switch Pin of converter 2. Connected to Inductor.
EN_DCDC1	20	I	Enable Input for converter 1, active high
EN_DCDC2	21	I	Enable Input for converter 2, active high
VINLDO1	2	I	Input voltage for LDO1
VINLDO2/3	8	I	Input voltage for LDO2 and LDO3
VLDO1	3	O	Output voltage of LDO1
VLDO2	7	O	Output voltage of LDO2
VLDO3	9	O	Output voltage of LDO3
DEF_DCDC2	5	I	Switches output voltages at DCDC2, logic high = 1.8V, logic low = 1.2V
DEF_LDO	4	I	Switches output voltages at LDO1, logic high = 3.3V, logic low = 3.3V Switches output voltages at LDO2, logic high = 1.8V, logic low = 1.2V Switches output voltages at LDO3, logic high = 1.8V, logic low = 1.3V
EN_LDO1	22	I	Enable input for LDO1. Logic high enables the LDO, logic low disables the LDO.
EN_LDO2	11	I	Enable input for LDO2. Logic high enables the LDO, logic low disables the LDO.
EN_LDO3	12	I	Enable input for LDO3. Logic high enables the LDO, logic low disables the LDO.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
$\overline{\text{RESET}}$	10	O	Open drain active low reset output, 100ms reset delay time after both DCDC1 and DCDC2 are within 95% of nominal output voltage (see Reset Generation and Output Monitoring section)
PowerPAD™	–		Connect to GND

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

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EFFICIENCY CONVERTER 1 vs LOAD CURRENT PWM/PFM MODE

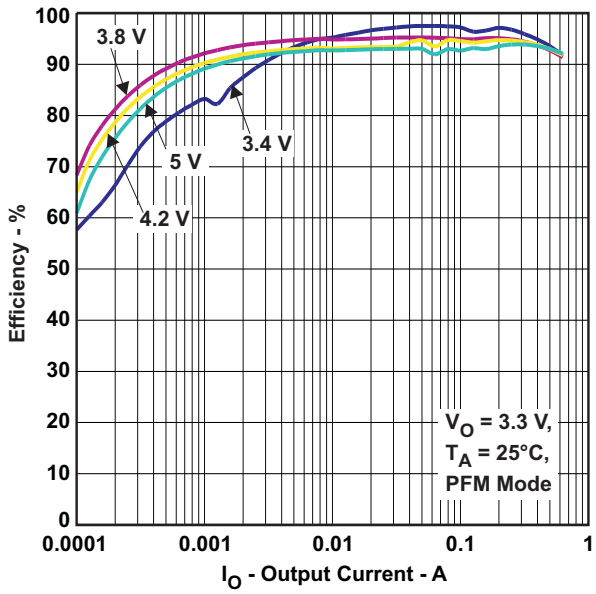


Figure 1.

EFFICIENCY CONVERTER 1 vs LOAD CURRENT PWM MODE

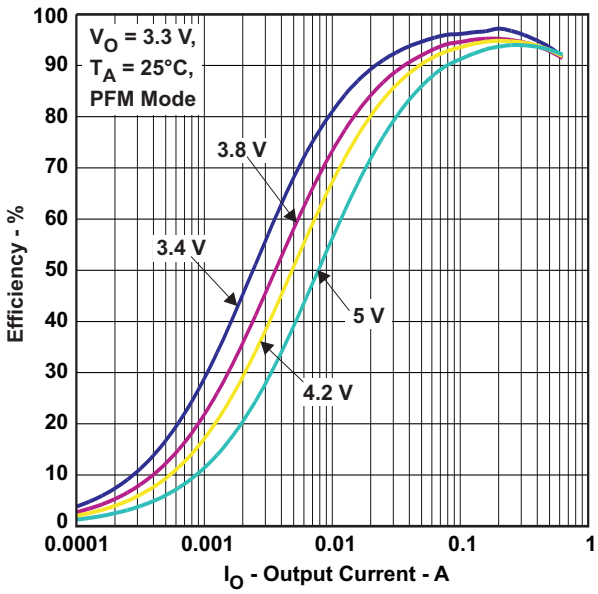


Figure 2.

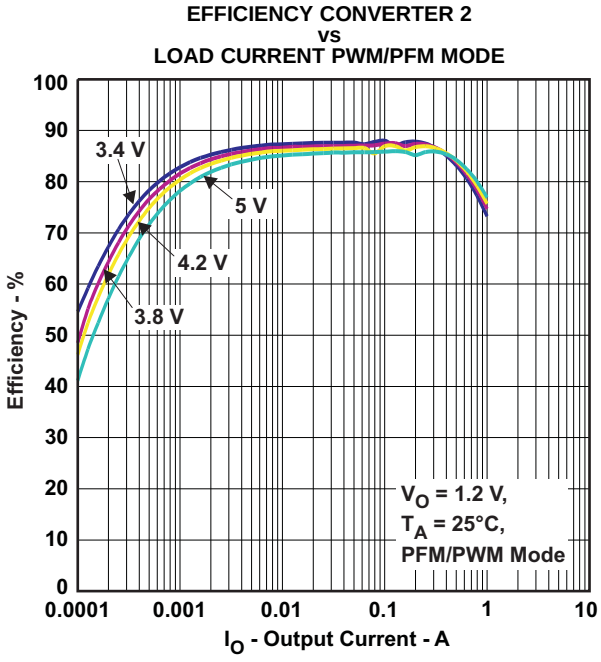


Figure 3.

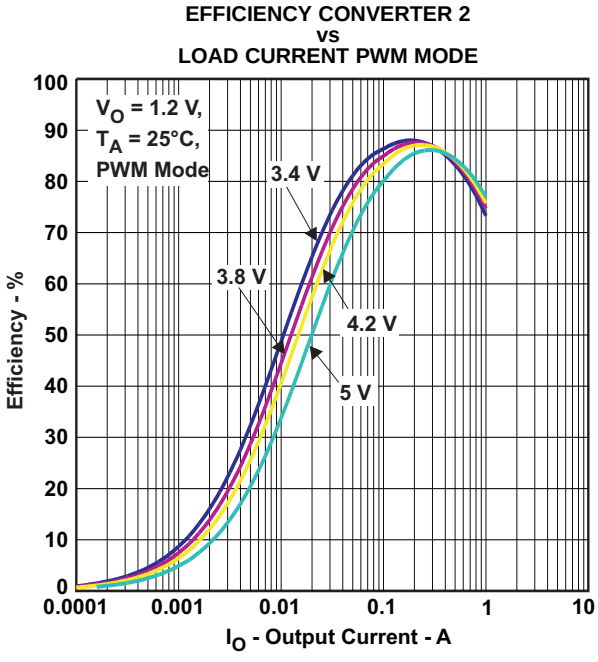


Figure 4.

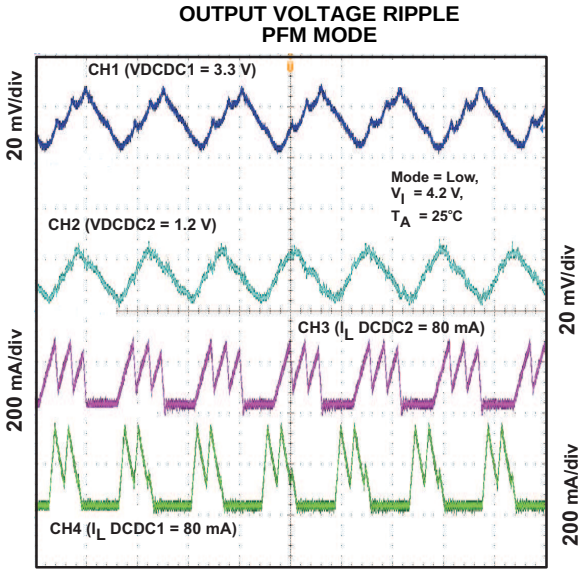


Figure 5.

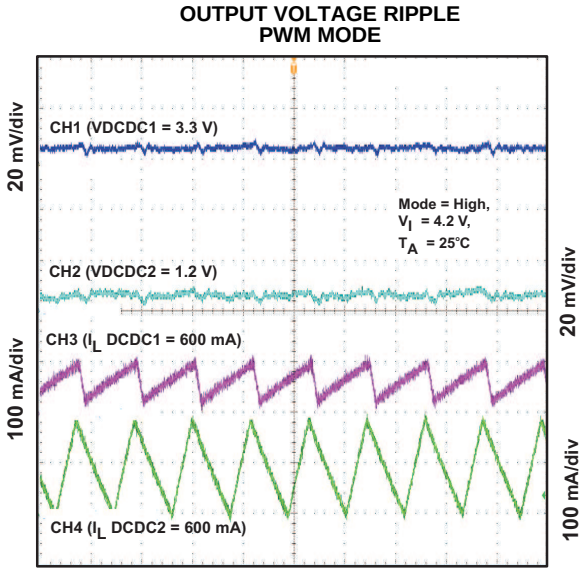
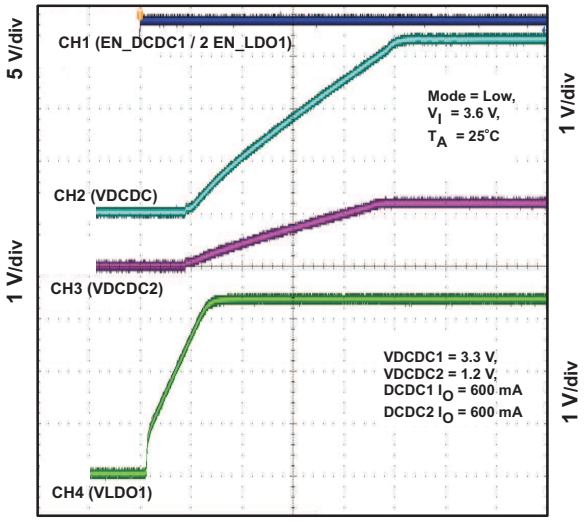


Figure 6.

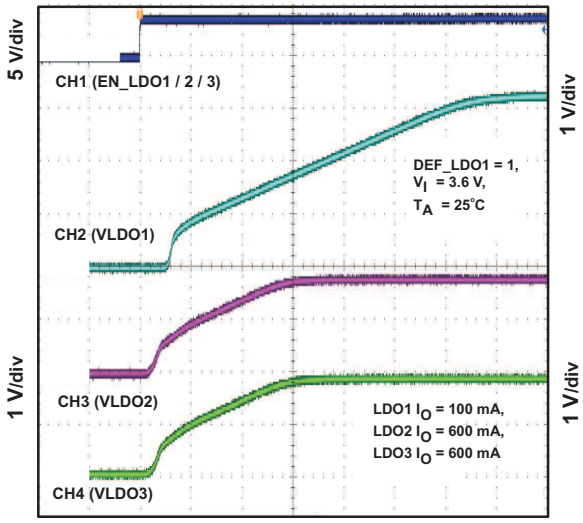
STARTUP CONVERTER 1 AND 2



t – Time = 200 µs/div

Figure 7.

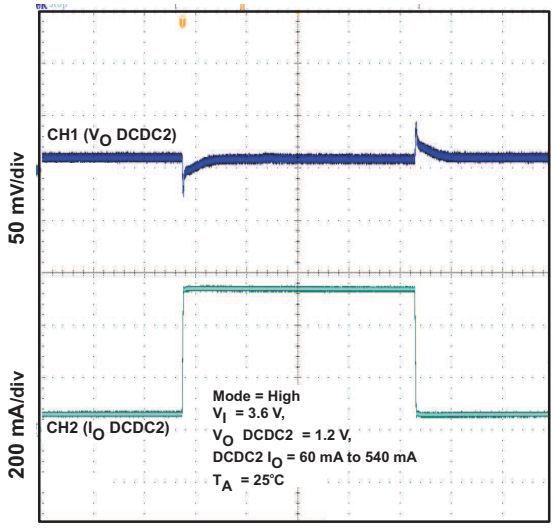
STARTUP LDO1 TO LDO3



t – Time = 40 µs/div

Figure 8.

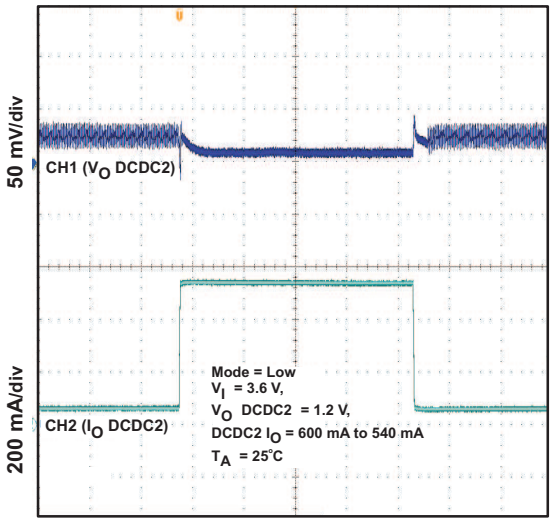
LOAD TRANSIENT RESPONSE
CONVERTER 2 IN PWM MODE



t – Time = 100 µs/div

Figure 9.

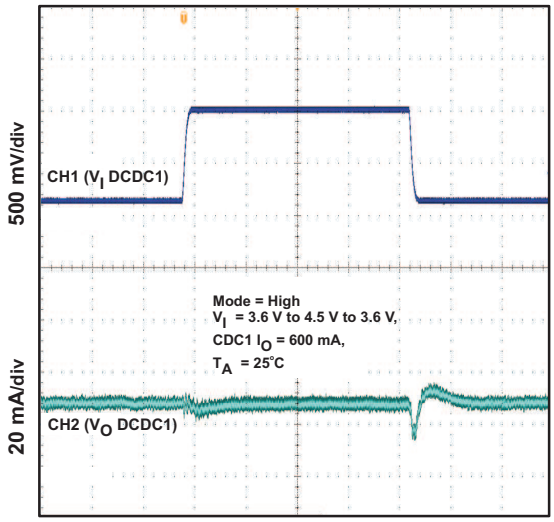
LOAD TRANSIENT RESPONSE
CONVERTER 2 IN PFM MODE



t – Time = 100 µs/div

Figure 10.

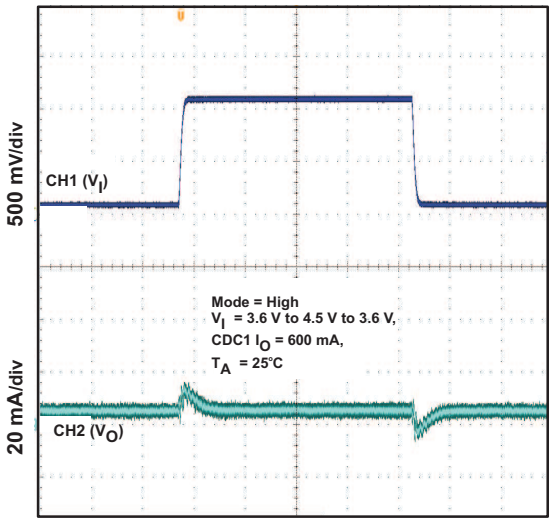
LINE TRANSIENT RESPONSE
CONVERTER 1



t − Time = 100 μs/div

Figure 11.

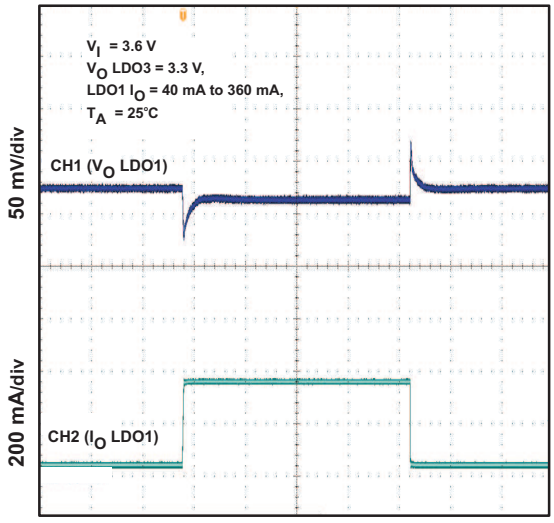
LINE TRANSIENT RESPONSE
CONVERTER 2



t − Time = 100 μs/div

Figure 12.

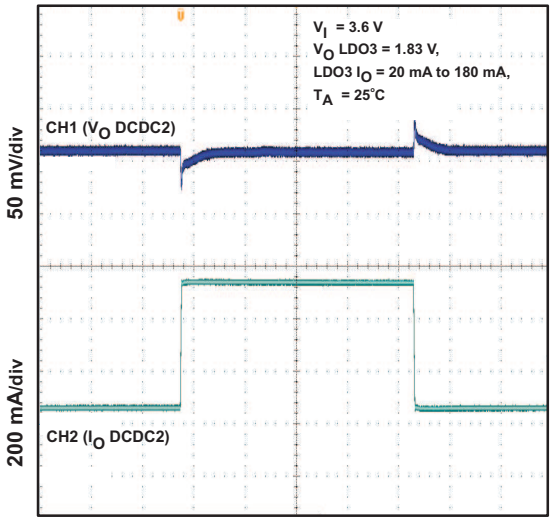
LOAD TRANSIENT RESPONSE
LDO1



t − Time = 100 μs/div

Figure 13.

LOAD TRANSIENT RESPONSE
LDO2 AND LDO3



t − Time = 100 μs/div

Figure 14.

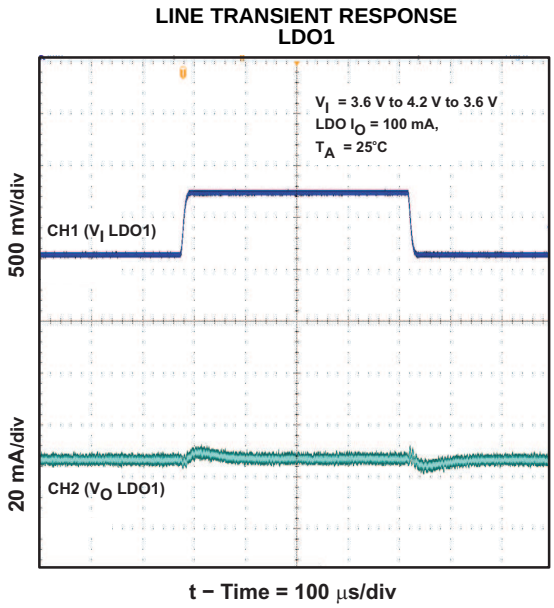


Figure 15.

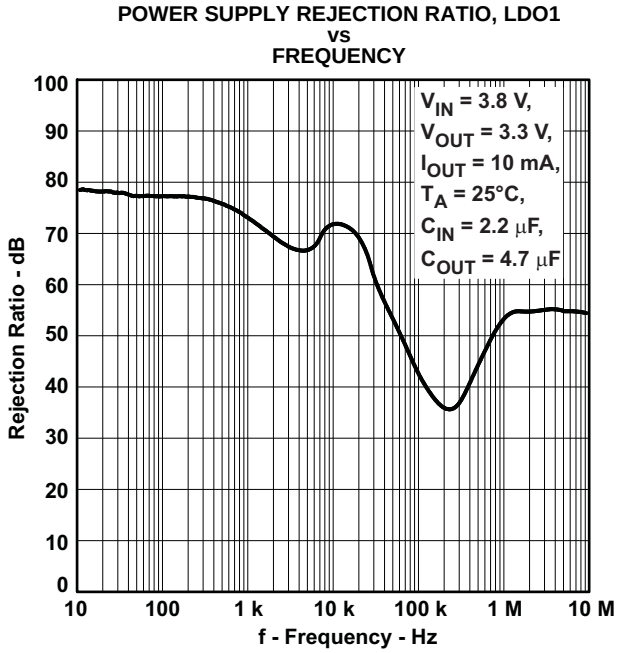


Figure 16.

DETAILED DESCRIPTION

OPERATION

The TPS65058 includes two synchronous step-down converters. The converters operate with 2.25MHz fixed frequency pulse width modulation (PWM) at moderate to heavy load currents. At light load currents, the converters automatically enter Power Save Mode and operate with PFM (Pulse Frequency Modulation).

During PWM operation, the converters use a unique fast response voltage mode controller scheme with input voltage feed-forward to achieve good line and load regulation allowing the use of small ceramic input and output capacitors. At the beginning of each clock cycle initiated by the clock signal, the P-channel MOSFET switch is turned on and the inductor current ramps up until the comparator trips and the control logic turns off the switch. The current limit comparator will also turn off the switch in case the current limit of the P-channel switch is exceeded. After the adaptive dead time prevents shoot through current, the N-channel MOSFET rectifier is turned on and the inductor current ramps down. The next cycle is initiated by the clock signal again turning off the N-channel rectifier and turning on the P-channel switch.

The two DC-DC converters operate synchronized to each other, with converter 1 as the master. A 180° phase shift between Converter 1 and Converter 2 decreases the input RMS current. Therefore smaller input capacitors can be used.

The converters output voltage is set by an external resistor divider connected to FB_DCDC1 or FB_DCDC2, respectively. See application section for more details.

POWER SAVE MODE

The Power Save Mode is enabled with Mode Pin set to low. If the load current decreases, the converters will enter Power Save Mode operation automatically. During Power Save Mode the converters operate with reduced switching frequency in PFM mode and with a minimum quiescent current to maintain high efficiency. The converter will position the output voltage typically 1% above the nominal output voltage. This voltage positioning feature minimizes voltage drops caused by a sudden load step.

In order to optimize the converter efficiency at light load the average current is monitored and if in PWM mode the inductor current remains below a certain threshold, then Power Save Mode is entered. The typical threshold can be calculated according to:

Equation 1: Average output current threshold to enter PFM mode.

$$I_{PFM\_enter} = \frac{VIN_{DCDC}}{32\ \Omega} \quad (1)$$

Equation 2: Average output current threshold to leave PFM mode.

$$I_{PFM\_leave} = \frac{VIN_{DCDC}}{24\ \Omega} \quad (2)$$

During the Power Save Mode the output voltage is monitored with a comparator. As the output voltage falls below the skip comparator threshold (skip comp) of $V_{OUTnominal}$ +1%, the P-channel switch will turn on and the converter effectively delivers a constant current as defined above. If the load is below the delivered current then the output voltage will rise until the same threshold is crossed again, whereupon all switching activity ceases, hence reducing the quiescent current to a minimum until the output voltage has dropped below the threshold again. If the load current is greater than the delivered current then the output voltage will fall until it crosses the skip comparator low (Skip Comp Low) threshold set to 1% below nominal Vout, whereupon Power Save Mode is exited and the converter returns to PWM mode.

These control methods reduce the quiescent current typically to 12µA per converter and the switching frequency to a minimum thereby achieving the highest converter efficiency. The PFM mode operates with very low output voltage ripple. The ripple depends on the comparator delay and the size of the output capacitor; increasing capacitor values will make the output ripple tend to zero.

The Power Save Mode can be disabled by driving the MODE pin high. Both converters will operate in fixed PWM mode. Power Save Mode Enable/Disable applies to both converters.

Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It is activated in Power Save Mode operation when the converter runs in PFM Mode. It provides more headroom for both the voltage drop at a load step increase and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converters operate in PFM Mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage will drop until it reaches the skip comparator low threshold set to –1% below the nominal value and enters PWM mode. During a load throw off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the N-channel switch.

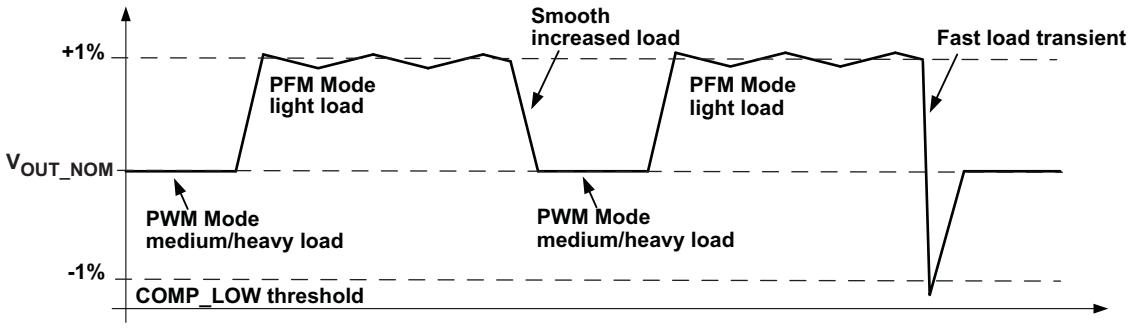


Figure 17. Dynamic Voltage Positioning

Soft Start

The two converters have an internal soft start circuit that limits the inrush current during start-up. During soft start, the output voltage ramp up is controlled as shown in Figure 18.

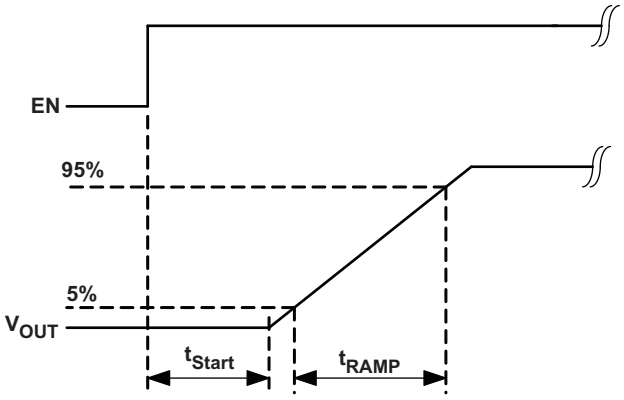


Figure 18. Soft Start

100% Duty Cycle Low Dropout Operation

The converters offer a low input to output voltage difference while still maintaining operation with the use of the 100% duty cycle mode. In this mode the P-channel switch is constantly turned on. This is particularly useful in battery-powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range, i.e. The minimum input voltage to maintain regulation depends on the load current and output voltage and can be calculated as:

$$V_I min = V_{OUT} max + I_{OUT} max \times (R_{DS(on)max} + R_L)$$

with:

I_{OUT}max = maximum output current plus inductor ripple current
$R_{DS(on)}$max = maximum P-channel switch $r_{DS(on)}$
R_L = DC resistance of the inductor
V_{OUT}max = nominal output voltage plus maximum output voltage tolerance

With decreasing load current, the device automatically switches into pulse skipping operation in which the power stage operates intermittently based on load demand. By running cycles periodically the switching losses are minimized and the device runs with a minimum quiescent current maintaining high efficiency.

In power save mode, the converter only operates when the output voltage trips below its nominal output voltage. It ramps up the output voltage with several pulses and goes again into power save mode once the output voltage exceeds the nominal output voltage.

Undervoltage Lockout

The undervoltage lockout circuit prevents the device from malfunctioning by disabling the converter at low input voltages and from excessive discharge of the battery. The undervoltage lockout threshold is typically 1.8 V, max 2 V.

MODE SELECTION

The MODE pin allows mode selection between forced PWM Mode and power Save Mode for both converters. Connecting this pin to GND enables the automatic PWM and power save mode operation. The converters operate in fixed frequency PWM mode at moderate to heavy loads and in the PFM mode during light loads, maintaining high efficiency over a wide load current range.

Pulling the MODE pin high forces both converters to operate constantly in the PWM mode even at light load currents. The advantage is the converters operate with a fixed frequency that allows simple filtering of the switching frequency for noise sensitive applications. In this mode, the efficiency is lower compared to the power save mode during light loads. For additional flexibility it is possible to switch from power save mode to forced PWM mode during operation. This allows efficient power management by adjusting the operation of the converter to the specific system requirements.

ENABLE

The device has a separate enable pin for each dcdc converter and for each LDO to start up each converter independently. If EN_DCDC1, EN_DCDC2, EN_LDO1, EN_LDO2, EN_LDO3 are set to high, the corresponding converter starts up with soft start as previously described.

Pulling the enable pin low forces the device into shutdown, with a shutdown quiescent current as defined in the electrical characteristics. In this mode, the P and N-Channel MOSFETs are turned-off, the and the entire internal control circuitry is switched-off. If disabled, the outputs of the LDOs are pulled low by internal 300Ω resistors, actively discharging the output capacitor. For proper operation, the enable pins must be terminated and must not be left unconnected.

OUTPUT VOLTAGE SELECTION

The output voltage of the DCDC Converter 2 can be selected by a logic level on pin DEF_DCDC2. The output voltage can be changed dynamically during operation. The slew rate of the change of output voltage is controlled on DCDC2 to be 9.6mV/µs.

The output voltages on the LDOs can also be changed dynamically between two voltages by changing the logic level on pin DEF_LDO.

The output voltage options are:

Table 1. Output Voltage Selection

DEF_LDO	1	0
LDO1	3.3 V	3.3 V
LDO2	1.8 V	1.2 V
LDO3	1.8 V	1.3 V
DEF_DCDC2	**1**	**0**
DCDC2	1.8 V	1.2 V

RESET GENERATION AND OUTPUT MONITORING

The TPS65058 contains a monitor circuitry that monitors the outputs of the DCDC converters and applies a reset pulse to the RESET pin. As soon as the supply voltage on the VCC pin is above the undervoltage lockout threshold, the RESET pin is pulled low. After the enabling of both DCDC converters, the output voltages are monitored. When both outputs are within 95% of the desired output voltage, the reset timer is started and after a delay of 100ms the Reset output is switched to high impedance. If one of the output voltages is outside of the regulation band (90% of the desired value) the RESET pin remains to be pulled to ground. After both outputs are back in regulation, the 100ms timer is started, and after 100ms the RESET output is again switched to high impedance.

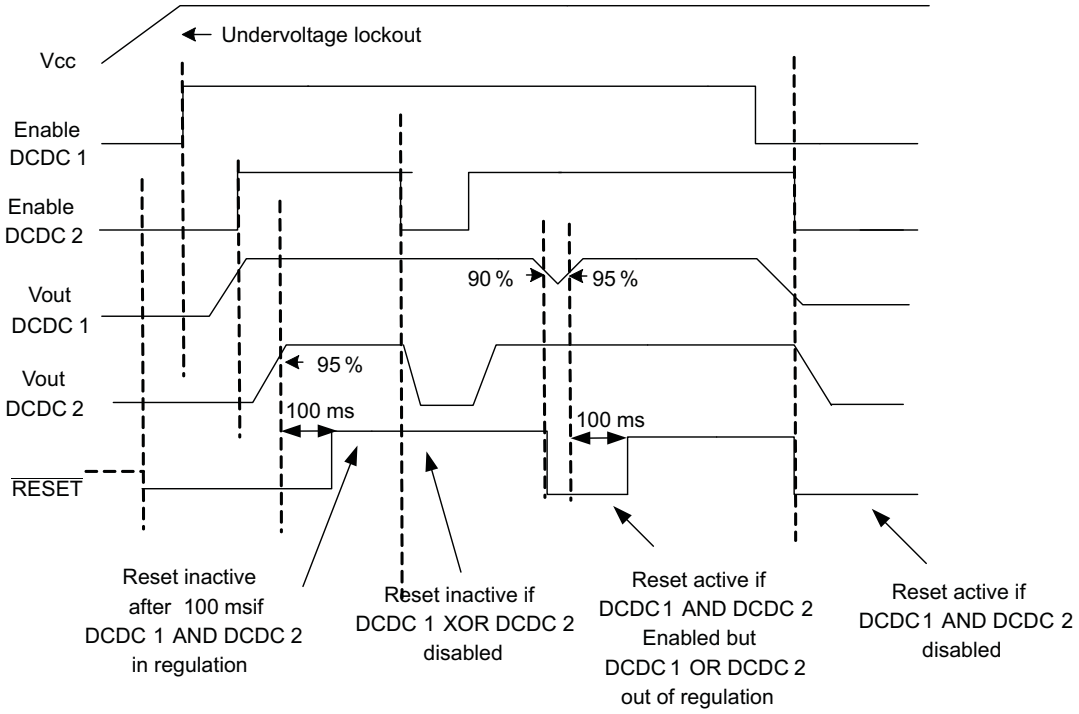


Figure 19. RESET Pulse Circuit

SHORT-CIRCUIT PROTECTION

All outputs are short circuit protected with a maximum output current as defined in the Electrical Characteristics.

THERMAL SHUTDOWN

As soon as the junction temperature, T_J, exceeds typically 150°C for the DCDC converters, the device goes into thermal shutdown. In this mode, the P and N-Channel MOSFETs are turned-off. The device continues its operation when the junction temperature falls below the thermal shutdown hysteresis again. A thermal shutdown for one of the DCDC converters will disable both converters simultaneously.

The thermal shutdown temperature for the LDOs are set to typically 140°C. Therefore, a LDO which is used to power an external voltage will never heat up the chip to a temperature high enough to turn off the DCDC converters. If one LDO exceeds the thermal shutdown temperature, all LDOs will turn off simultaneously.

Low Dropout Voltage Regulators

The low dropout voltage regulators are designed to operate with low value ceramic input and output capacitors. They operate with input voltages down to 1.5V. The LDOs offer a maximum dropout voltage of 280mV at rated output current. Each LDO supports a current limit feature. The LDOs are enabled by the EN_LDO1, ENLDO2, and EN_LDO3 pin. The output voltage of LDO1, LDO2 and LDO3 can be selected by the DEF_LDO pin according to Table 1.

For noise and stability reasons, X5R or X7R type ceramic capacitors are recommended to limit degeneration of °C over temperature and Vout.

OUTPUT FILTER DESIGN (INDUCTOR AND OUTPUT CAPACITOR)

Inductor Selection

The two converters operate typically with 2.2µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. For output voltages higher than 2.8V, an inductor value of 3.3µH minimum should be selected, otherwise the inductor current will ramp down too fast causing imprecise internal current measurement, and therefore, increased output voltage ripple under some operating conditions in PFM mode.

The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance will directly influence the efficiency of the converter. Therefore, an inductor with lowest DC resistance should be selected for highest efficiency.

Equation 4 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{out}max + \frac{\Delta I_L}{2} \tag{4}$$

with:

f = Switching Frequency (2.25 MHz typical)

L = Inductor Value

ΔI_L = Peak to Peak inductor ripple current

I_{Lmax} = Maximum Inductor current

The highest inductor current will occur at maximum Vin.

Open core inductors have a soft saturation characteristic, and usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. A consideration to be considered is that the core material from inductor to inductor differs, and has an impact on the efficiency, especially at high switching frequencies.

See Table 2 and the typical applications for possible inductors.

Table 2. Tested Inductors

INDUCTOR TYPE	INDUCTOR VALUE	SUPPLIER
LPS3010	2.2 µH	Coilcraft
LPS3015	3.3 µH	Coilcraft
LPS4012	2.2 µH	Coilcraft
VLF4012	2.2 µH	TDK

Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the two converters allow the use of small ceramic capacitors with a typical value of 22µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are recommended. SeeTable 3 for recommended components.

If ceramic output capacitors are used, the capacitor RMS ripple current rating will always meet the application requirements. Just for completeness the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (5)$$

At nominal load, current the inductive converters operate in PWM mode. The overall output voltage ripple is the sum of the voltage spike, caused by the output capacitor ESR plus the voltage ripple, caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (6)$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents, the converters operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

Input Capacitor Selection

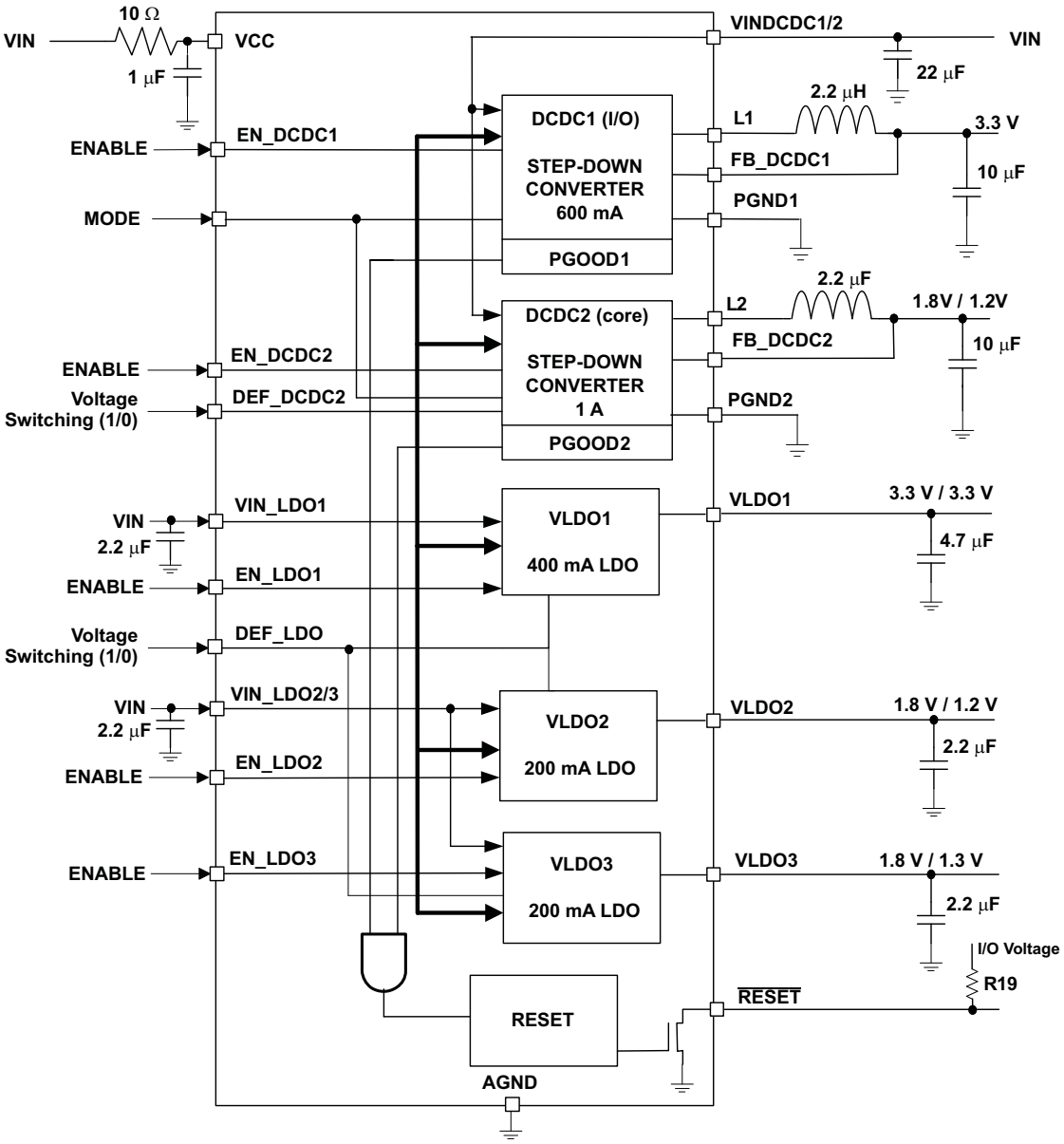
Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering, and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10µF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 3. Possible Capacitors

22 µF	0805	TDK C2012X5R0J226MT	Ceramic
22 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10uF	0805	TDK C2012X5R0J106M	Ceramic

APPLICATION INFORMATION

TYPICAL APPLICATION CIRCUIT



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS65058RGER	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65058RGERG4	ACTIVE	VQFN	RGE	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65058RGET	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS65058RGETG4	ACTIVE	VQFN	RGE	24	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

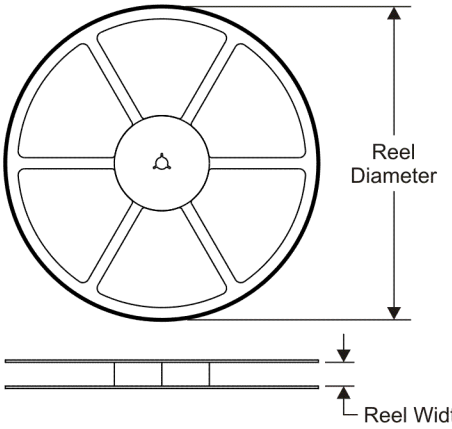
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

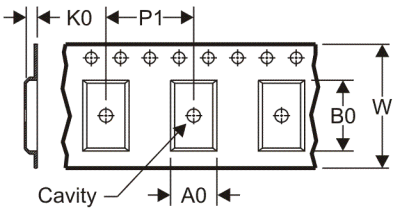
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

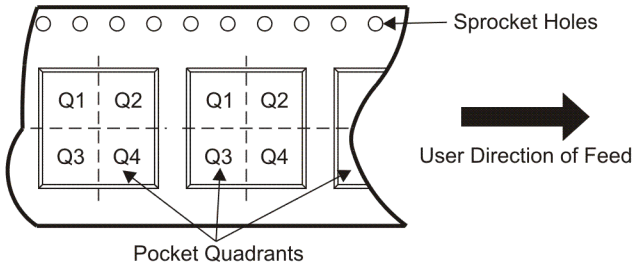


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

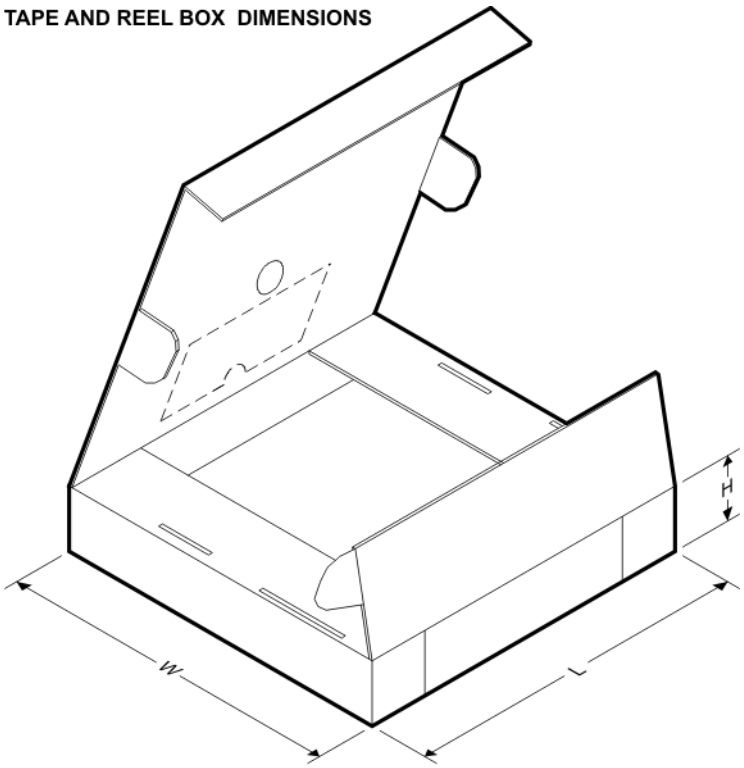
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65058RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TPS65058RGET	VQFN	RGE	24	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

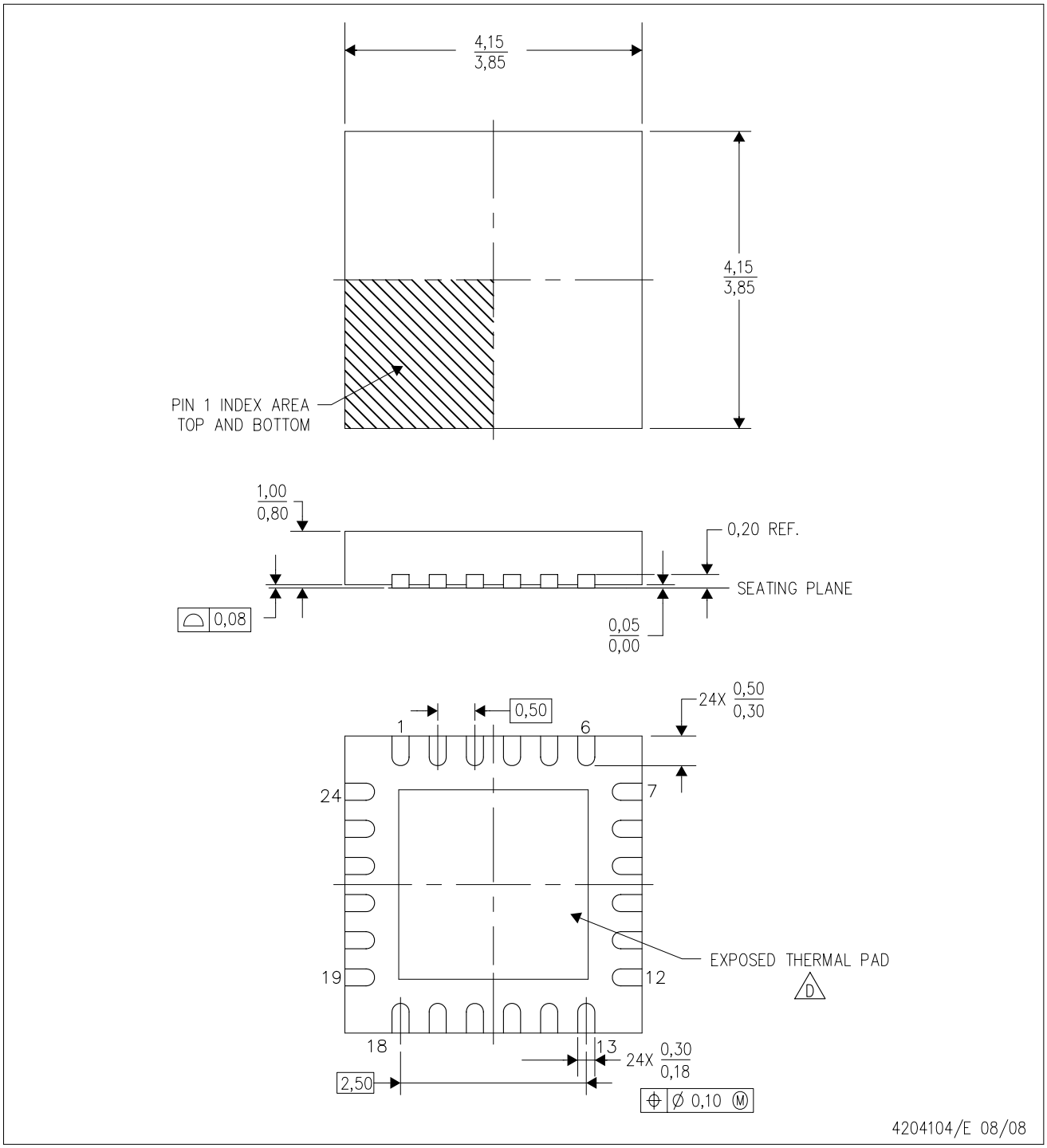
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65058RGER	VQFN	RGE	24	3000	346.0	346.0	29.0
TPS65058RGET	VQFN	RGE	24	250	190.5	212.7	31.8

RGE (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MO–220.

THERMAL PAD MECHANICAL DATA

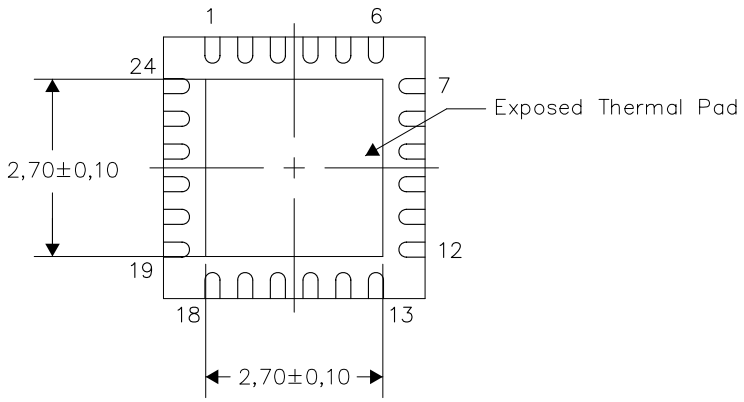
RGE (S–PVQFN–N24)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

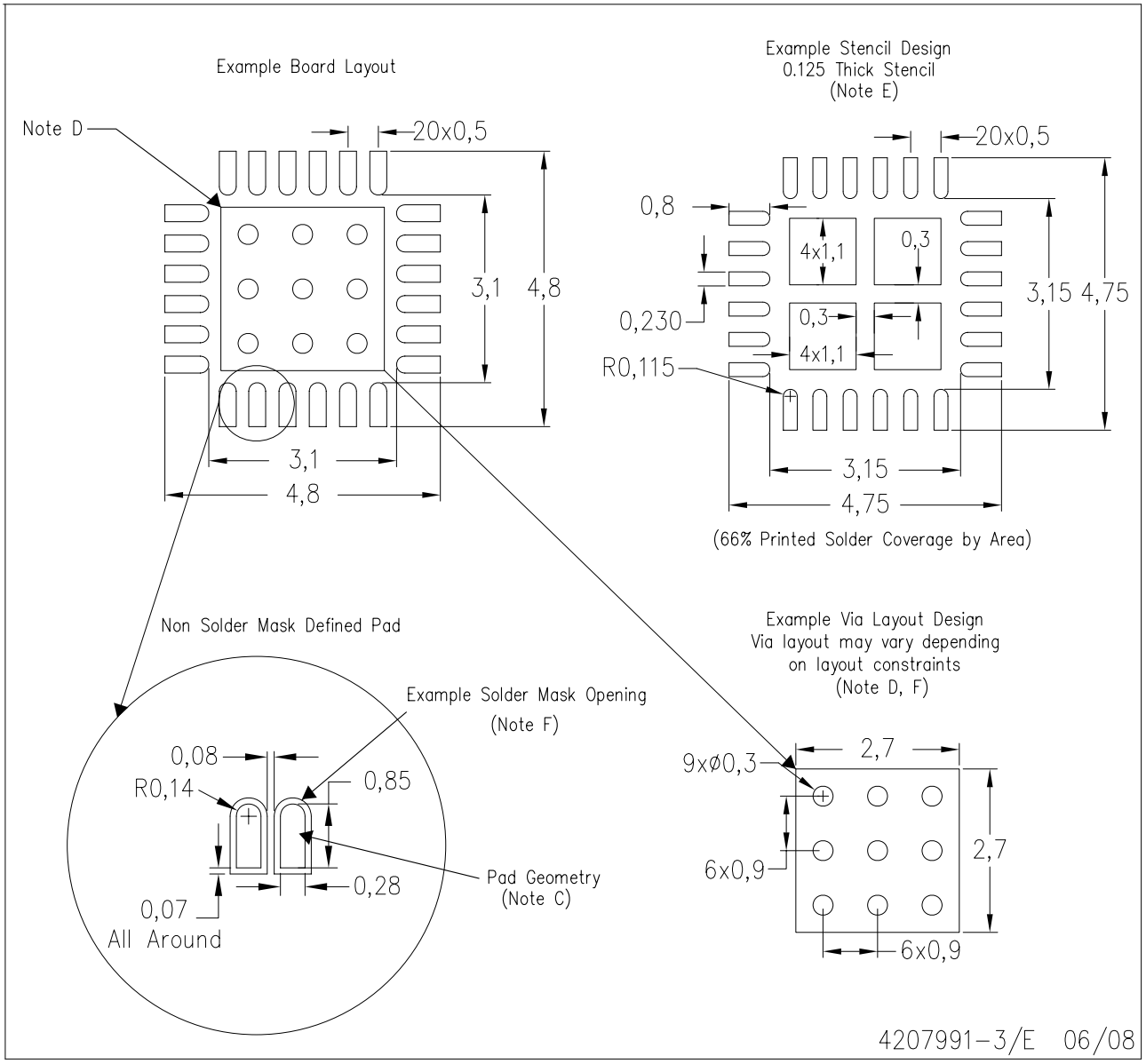


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

RGE (S–PVQFN–N24)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
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